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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Thornley et al.

Assignee: ZiLOG, Inc.

Title: "Circuit for Detection of Hardware Faults Due to Temporary Power Supply Fluctuations"

Serial No.: 10/750,232 Filed: December 29, 2003

Patent No.: 6,954,083 B1 Issued: October 11, 2005

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November 1, 2005

ATTN: Certificate of Correction Branch
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REQUEST FOR CERTIFICATE OF CORRECTION

Pursuant to 37 CFR 1.322, Applicants request that the Director issue a certificate of correction to correct mistakes in the printing of the above-identified patent incurred through the fault of the Patent Office. Mistakes in the printing of claims 15 and 18-20 are clearly apparent when the two attached pages of USP 6,954,083 (marked to show the mistakes) are compared to the two attached pages of the Listing of Claims that were submitted on April 21, 2005, along with a Response to the last office action. Text of the requested correction is submitted on the attached two pages of Certificate of Correction form, PTO/SB/44.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: ATTN: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By Darien K. Wallace
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Date of Deposit: November 1, 2005

Respectfully submitted,

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13. (original) The integrated circuit of Claim 11, further comprising:

a processor; and

a status register having a bit, wherein the bit is set by hardware if the fault output signal is output by the logic tree, and wherein the processor can read the bit of the register.

14. (original) The integrated circuit of Claim 13, wherein the reset signal generated by the reset circuit does not reset the bit in the status register.

15. (currently amended) An integrated circuit comprising:

a plurality of fast electromagnetic transient (EFT) fault detector ~~circuits~~, the plurality of the EFT fault detector ~~circuits~~ being distributed across at least a portion of the integrated circuit, wherein each of the EFT fault detector ~~circuits~~ outputs a signal indicative of whether said each EFT fault detector ~~circuit~~ has detected an EFT fault; and

a logic tree that receives the signals output from the plurality of EFT fault detector ~~circuits~~, the logic tree outputting a fault output signal, the fault output signal being indicative of whether any of the EFT fault detector ~~circuits~~ of the plurality of EFT fault detectors ~~circuit~~ has detected an EFT fault.

16. (original) The integrated circuit of Claim 15, wherein the fault output signal is not supplied as an input signal to a reset circuit on the integrated circuit.

17. (original) The integrated circuit of Claim 15, further comprising:

a reset circuit, wherein the fault output signal is supplied as an input signal to the reset circuit.

18. (currently amended) The integrated circuit of Claim 15, wherein the integrated circuit further comprises a reset circuit that outputs a reset signal if the reset circuit detects an out-of-specification voltage present between a power

supply lead on the integrated circuit and a ground lead on the integrated circuit, and wherein the reset circuit fails to detect an out-of-specification voltage if a two thousand volt spike is present between the power supply lead and the ground lead for less than two hundred nanoseconds, and wherein at least one of the EFT fault detector ~~circuit~~s detects the presence of the spike and in response thereto outputs the signal indicative of the EFT fault detector having detected the presence of an EFT fault.

19. (currently amended) The integrated circuit of Claim 15, wherein the integrated circuit is a standard cell integrated circuit, and wherein each of the EFT fault detector ~~circuit~~s is realized in the form of standard cell circuitry.

20. (currently amended) The integrated circuit of Claim 15, wherein the integrated circuit is a programmable logic device (PLD), the PLD comprising a plurality of logic blocks and a programmable interconnect structure, and wherein each of the plurality of ~~fast electromagnetic transient (~~EFT~~)~~ fault detector ~~circuit~~s is realized in the form of logic block circuitry.

21. (currently amended) An integrated circuit, comprising:

a first means for detecting a fast electromagnetic transient (EFT) fault having a duration less than two hundred nanoseconds;

a second means for detecting an EFT fault; and

a logic tree that receives signals from the first and second means and that outputs a fault detect signal indicative of whether either the first means or the second means has detected an EFT fault.

22. (currently amended) ~~The integrated circuit of Claim 21, further comprising:~~An integrated circuit, comprising:

a first means for detecting a fast electromagnetic transient (EFT) fault having a duration less than two hundred nanoseconds;

content of one or more of the flip-flops is determined to have changed, then an EFT fault signal is generated. The flip-flops of a JTAG register may, in some embodiments, be used to form a shift register that performs an EFT detection function. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the claims.

What is claimed is:

1. An integrated circuit comprising:

a plurality of digital logic storage elements, each of the digital logic storage elements being initialized to store a first digital logic value, each digital logic storage element being controlled after it is initialized such that it continues to store the first digital logic value throughout a period if the integrated circuit is powered from a supply voltage that remains within a normal operating supply voltage range, wherein each digital logic storage element outputs an output signal indicative of whether the digital logic storage element is storing a second digital logic value;

a logic tree that receives the output signals from said plurality of digital logic storage elements, the logic tree outputting a fault output signal; and

a reset circuit that receives the fault output signal from the logic tree, the reset circuit generating a reset signal if the output signal of any of the plurality of digital logic storage elements indicates that the corresponding digital logic storage element is storing said second digital logic value during said period.

2. The integrated circuit of claim 1, wherein the first digital logic value is a digital logic high, wherein said second digital logic value is a digital logic low, wherein the reset circuit generates the reset signal if any of the plurality of digital logic storage elements switches during said period from storing the first digital logic value to storing the second digital logic value.

3. The integrated circuit of claim 1, wherein the digital logic storage element is a flip-flop having a clear input lead, wherein the digital logic storage element is initialized by applying a clear signal to the clear input lead, and wherein during said period the clear signal is not present on the clear input lead.

4. The integrated circuit of claim 1, wherein the digital logic storage element is a flip-flop having a preset input lead, wherein the digital logic storage element is initialized by applying a preset signal to the preset input lead, and wherein during said period the preset signal is not present on the preset input lead.

5. The integrated circuit of claim 1, further comprising:

a circuit being monitored, wherein the integrated circuit comprises a first set of standard cells and a second set of standard cells, wherein standard cells of the first set are interconnected to form the circuit being monitored, and wherein the plurality of digital logic storage elements are digital logic storage elements of the second set of standard cells.

6. The integrated circuit of claim 3, wherein the plurality of digital logic storage elements are distributed across the integrated circuit such that at least some of the digital logic storage elements are islands surrounded by the circuit being monitored.

7. The integrated circuit of claim 1, wherein the digital logic storage element is a flip-flop, and wherein the digital logic storage element is controlled after it is initialized and throughout said period by: 1) not clocking the digital logic storage element, 2) not clearing the digital logic storage element, and 3) not presetting the digital logic storage element.

8. The integrated circuit of claim 1, further comprising:

a circuit being monitored, wherein the circuit being monitored comprises digital logic storage elements, and wherein the digital logic storage elements of the circuit being monitored are less susceptible to fast electromagnetic transients (EFT) than are the digital logic storage elements of the plurality of digital logic storage elements.

9. The integrated circuit of claim 1, wherein the integrated circuit is a standard cell integrated circuit, and wherein the reset circuit is a power-on reset circuit.

10. The integrated circuit of claim 1, wherein the logic tree consists only of combinatorial logic, and wherein the logic tree performs a logical OR function.

11. The integrated circuit of claim 1, wherein the reset circuit monitors the supply voltage and generates the reset signal if the supply voltage is detected to be outside the normal operating supply voltage range, but wherein the reset circuit does not detect the supply voltage being outside the normal operating supply voltage range if the supply voltage spikes above the normal operating supply range for an isolated time period of less than two hundred nanoseconds.

12. The integrated circuit of claim 11, further comprising:

a status register having a first bit and a second bit, the first bit being set by the reset circuit if the reset circuit detects the supply voltage being outside the normal operating supply voltage range, the second bit being set if the logic tree outputs the fault output signal to the reset circuit.

13. The integrated circuit of claim 11, further comprising:

a processor; and

a status register having a bit, wherein the bit is set by hardware if the fault output signal is output by the logic tree, and wherein the processor can read the bit of the register.

14. The integrated circuit of claim 13, wherein the reset signal generated by the reset circuit does not reset the bit in the status register.

15. An integrated circuit comprising:

a plurality of fast electromagnetic transient (EFT) fault detectors, the plurality of the EFT fault detectors being distributed across at least a portion of the integrated circuit, wherein each of the EFT fault detectors outputs a signal indicative of whether said each EFT fault detector has detected an EFT fault; and

a logic tree that receives the signals output from the plurality of EFT fault detectors, the logic tree outputting a fault output signal, the fault output signal being indicative of whether any of the EFT fault detectors of the plurality of EFT fault detectors has detected an EFT fault.

16. The integrated circuit of claim 15, wherein the fault output signal is not supplied as an input signal to a reset circuit on the integrated circuit.

17. The integrated circuit of claim 15, further comprising:

a reset circuit, wherein the fault output signal is supplied as an input signal to the reset circuit.

18. The integrated circuit of claim 15, wherein the integrated circuit further comprises a reset circuit that outputs a reset signal if the reset circuit detects an out-of-specification voltage present between a power supply lead on the integrated circuit and a ground lead on the integrated circuit, and wherein the reset circuit fails to detect an out-of-specification voltage if a two thousand volt spike is present between

the power supply lead and the ground lead for less than two hundred nanoseconds, and wherein at least one of the EFT fault detectors detects the presence of the spike and in response thereto outputs the signal indicative of the EFT fault detector having detected the presence of an EFT fault.

19. The integrated circuit of claim **15**, wherein the integrated circuit is a standard cell integrated circuit, and wherein each of the EFT fault detectors is realized in the form of standard cell circuitry.

20. The integrated circuit of claim **15**, wherein the integrated circuit is a programmable logic device (PLD), the PLD comprising a plurality of logic blocks and a programmable interconnect structure, and wherein each of the plurality of EFT fault detectors is realized in the form of logic block circuitry.

21. An integrated circuit, comprising:

a first means for detecting a fast electromagnetic transient (EFT) fault having a duration less than two hundred nanoseconds;

a second means for detecting an EFT fault; and

a logic tree that receives signals from the first and second means and that outputs a fault detect signal indicative of whether either the first means or the second means has detected an EFT fault.

22. An integrated circuit, comprising:

a first means for detecting a fast electromagnetic transient (EFT) fault having a duration less than two hundred nanoseconds;

a second means for detecting an EFT fault;

a logic tree that receives signals from the first and second means and that outputs a fault detect signal indicative of whether either the first means or the second means has detected an EFT fault;

a first structure through which the integrated circuit receives a supply voltage, wherein the first means is located adjacent to the first structure; and

a second structure through which the integrated circuit is coupled to ground potential, wherein the second means is located adjacent to the second structure.

23. A method, comprising:

providing a plurality of detectors in an integrated circuit, wherein each of said detectors is capable of detecting a fast electromagnetic transient (EFT) fault having a duration less than two hundred nanoseconds; and

generating, on the integrated circuit, a signal indicative of whether any one of said plurality of detectors has detected an EFT fault.

24. The method of claim **23**, wherein each of said detectors is capable of detecting an EFT fault that occurs in the integrated circuit.

25. The integrated circuit of claim **21**, wherein the first means detects an EFT fault that occurs in the integrated circuit.

* * * * *

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,954,083 B1

APPLICATION NO.: 10/750,232

ISSUE DATE : October 11, 2005

INVENTOR(S) : Thornley et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, lines 44, 46, 50 and 52, "detector" should be changes to --detectors--.
Lines 42-54, claim 15 should read:

15. An integrated circuit comprising:
a plurality of fast electromagnetic transient (EFT) fault detectors, the plurality of the EFT fault detectors being distributed across at least a portion of the integrated circuit, wherein each of the EFT fault detectors outputs a signal indicative of whether said each EFT fault detector has detected an EFT fault; and
a logic tree that receives the signals output from the plurality of EFT fault detectors, the logic tree outputting a fault output signal, the fault output signal being indicative of whether any of the EFT fault detectors of the plurality of EFT fault detectors has detected an EFT fault.

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PATENT NO. : 6,954,083 B1

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ISSUE DATE : October 11, 2005

INVENTOR(S) : Thornley et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 11, lines 3, 8, and 14, "detector" should be changes to --detectors--.
Lines 1-15, claims 18-20 should read:

the power supply lead and the ground lead for less than two hundred nanoseconds, and wherein at least one of the EFT fault detectors detects the presence of the spike and in response thereto outputs the signal indicative of the EFT fault detector having detected the presence of an EFT fault.

19. The integrated circuit of Claim 15, wherein the integrated circuit is a standard cell integrated circuit, and wherein each of the EFT fault detectors is realized in the form of standard cell circuitry.

20. The integrated circuit of Claim 15, wherein the integrated circuit is a programmable logic device (PLD), the PLD comprising a plurality of logic blocks and a programmable interconnect structure, and wherein each of the plurality of EFT fault detectors is realized in the form of logic block circuitry.

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